AMENDMENTS TO THE CLAIMS

Claim 1 (original): In a three terminal silicon based metal insulator semiconductor (MIS) device, the improvement comprising:

a threshold voltage which can be controlled using a first control signal applied to a first terminal of the three terminal silicon based MIS device;

a negative differential resistance (NDR) mode which is enabled when said first control signal exceeds an NDR onset voltage associated with the three terminal silicon based MIS device and said threshold voltage is increased.

Claim 2 (original): The three terminal silicon based MIS device of claim 1, wherein said threshold voltage also is controlled using a second control signal applied to a gate terminal of the three terminal silicon based MIS device;

Claim 3 (original): The three terminal silicon based MIS device of claim 1, wherein the device is an n-channel transistor having a polysilicon gate.

Claim 4 (original): The three terminal silicon based MIS device of claim 1, wherein the NDR mode for such device can be disabled through a separate bias voltage applied to a fourth terminal for the device.

Claim 5 (original): The three terminal silicon based MIS device of claim 1, wherein said NDR onset voltage is set during a CMOS compatible manufacturing operation.

Claim 6 (original): The three terminal silicon based MIS device of claim 5, wherein said CMOS compatible manufacturing operation is an implant.

Claim 7 (original): The three terminal silicon based MIS device of claim 5, wherein said CMOS compatible manufacturing operation sets a channel length for such device.

Claim 8 (original): The three terminal silicon based MIS device of claim 5, wherein said NDR onset voltage can be reduced by reducing a channel length for such device.

Claim 9 (original): The three terminal silicon based MIS device of claim 1, wherein a peak-to-valley current ratio in said NDR mode is set during a CMOS compatible manufacturing operation.

Claim 10 (original): The three terminal silicon based MIS device of claim 1, wherein said device is used as a delay element.

Claim 11 (original): A method of operating a negative differential resistance (NDR) semiconductor transistor device, including the steps of:

(a) turning the NDR semiconductor transistor device on by applying a gate voltage which exceeds a threshold voltage for the NDR semiconductor transistor device;

(b) turning the NDR semiconductor transistor device off by applying a separate source-drain bias voltage which causes said threshold voltage to increase and reduce conduction in a channel region.

Claim 12 (original): The method of claim 11, wherein the NDR semiconductor transistor device can be turned on again after step (b) by altering said source-drain bias voltage to reduce said threshold voltage.

Claim 13 (original): A method of operating a silicon based n-channel semiconductor transistor device which includes a gate, a source region, a drain region, and a channel region coupling the source region and drain region, including the steps of:

turning on the silicon based n-channel semiconductor transistor device by applying a first gate bias voltage which exceeds a threshold voltage of the n-channel semiconductor transistor device;

varying said threshold voltage of the silicon based n-channel semiconductor transistor device;

turning off the silicon based n-channel semiconductor transistor device by applying a second source-drain bias voltage which causes said threshold voltage to exceed said first gate bias voltage;

wherein said threshold voltage can be varied so that the silicon based n-channel semiconductor transistor device has a channel current which exhibits negative differential resistance.

Claim 14 (original): A method of operating a semiconductor transistor device in a negative differential resistance mode comprising the steps of:

(a) biasing a channel region of the semiconductor transistor device with a first bias voltage so as to create a channel current that within a first operating region increases as said first bias voltage increases;

(b) trapping a number of carriers from said channel region in temporary trapping sites, said number being proportionate to a value of said first bias voltage so that within a second operating region said channel current decreases as said first bias voltage increases;

wherein the semiconductor transistor device operates with a negative differential resistance characteristic in said second operating region;

further wherein the semiconductor transistor device is configured as a delay device, with a time delay based on a trapping rate achieved by said temporary trapping sites.

Claim 15 (original): The method of claim 14, wherein said trapping rate is controlled by a value of said first bias voltage.

Claim 16 (original): The method of claim 14, wherein said trapping rate is controlled by a location of said temporary trapping sites.

Claim 17 (original): The method of claim 14, wherein said trapping rate is controlled by a semiconductor-insulator interface potential barrier associated with the semiconductor transistor device.

Claim 18 (original): The method of claim 14, wherein said trapping rate is adjusted by a CMOS processing operation during manufacturing of the semiconductor transistor device.

Claim 19 (original): The method of claim 14, wherein said carriers are energetic electrons trapped in a dielectric layer

adjacent to a channel region of the semiconductor transistor device.

Claim 20 (original): The method of claim 14, wherein said carriers do not include substantial numbers of hot holes.